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09/919,740	08/01/2001	Shauki Elassaad	21891.03100	3948
7590	03/15/2005		EXAMINER DINH, PAUL	
John W. Carpenter CROSBY, HEAFEY, ROACH & MAY P.O. Box 7936 San Francisco, CA 94120-7936			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/919,740

Applicant(s)

ELASSAAD ET AL.

Examiner

Paul Dinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 27 January 2005.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.  
4a) Of the above claim(s) 20-26 is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-9 and 13-19 is/are rejected.  
7) ☒ Claim(s) 10-12 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 01 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 5/28/03 + 11/17/03.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

- This is a response to the Applicant election filed on 1/27/05.
- The election of group I (a method of inserting buffer (claims 1-19 as best understood by the examiner since the applicant fails to identify claims belonging to group I)) with traverse is acknowledged.
- Because applicant did not address or point out any reasons/grounds/evidences/ explanations to support the traverse, the restriction, after being reconsidered by the examiner, is made final.
- The applicant is advised that cancellation of non-elected claims (group II (claims 20-26)) is required; the restriction is final.

### ***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. The following claims recite the following features:

(Claim 1) "placed macros";

(Claims 13-14) "computer" and "computer readable media".

Therefore, these features must be clearly shown in the drawings or this feature canceled from the claim(s).

**No new subject matter should be entered.**

### **Claim Objections**

Claim 6 is objected to because it seems that "D is the delay of the edge", "R is a resistance of the edge" and "C is a capacitance of the edge" should be changed to "D<sup>i</sup> is the delay of the edge", "R<sup>i</sup> is a resistance of the edge" and "C<sup>i</sup> is a capacitance of the edge", respectively.

Claims 16 and 18 is objected to because "can be" is not a positive of the invention and should not be used in the claim language.

### **Claim Rejections - 35 USC § 112**

*The following is a quotation of the first paragraph of 35 U.S.C. 112:*  
*The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

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Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 15 is rejected because “computer readable instructions stored in an electronic signal” find no clear support in the specification.

*The following is a quotation of the second paragraph of 35 U.S.C. 112:*

*The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.*

Claims 4-8, 15-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The following claims are rejected because:

- a. (Claim 4) “said step of calculating intervals” lack antecedent basis. Claims 5-8 are rejected because they depend on claim 4.
- b. (Claim 6) “the branch” lacks antecedent basis.
- c. (Claim 6-7, and 15) “branch” and “branches” are incomplete without defining branch/branches of what.
- d. (Claim 8) “the stage” and “the branch” lack antecedent basis.
- e. (Claim 8) “Cx<sup>i</sup>” is incomplete without “Cx<sup>i</sup>
- f. (Claim 15) It is not clear and it does not make sense as to how “instructions” are (or can be) “stored in a electronic signal”.
- g. (Claim 16) “the merged layer” (line 7-8) and “the merged edge” (line 11) lack antecedent basis. Claims 17-19 are rejected because they depend on claim 16.
- h. (Claim 16) It is not clear that “the segment” (line 11) referring to “merged segment” (line 4) or “staircase segment” line 6. Claims 17-19 are rejected because they depend on claim 16

#### ***Claim Rejections - 35 USC § 102***

*The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:*

*A person shall be entitled to a patent unless –*

*(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

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*(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

1. Claims 1-5, 7, 9, 13-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Alpert et al (US Patent Application No. 2002/0184607)

(Claims 1, 16-19)

preparing a physical hierarchy of the circuit design with placed macros (fig 1, 4-5);

performing global routing on the physical hierarchy (para 0006, 0009, 0012, 0035, 0047-0048, 0057);

determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets (para 0007, 0048);

calculating a position for each buffer (abstract, summary, para 0042, claim 1); and

inserting a buffer configured to boost timing performance at each calculated position (para 0005, 0007, 0043).

(Claims 2-3) wherein said buffers are inverters/repeaters (para 0004, 0036, 0047).

(Claims 4-5) identifying a set at least one edge in said nets for inserting buffers; and determining an optimal number of buffers to be inserted on each edge (fig 3-12), calculating, for each edge, the optimal number of buffers based on an optimal timing for the edge, a delay of the edge, and an impedance of the edge (fig 3-12).

(Claims 7, 9) determining a uniform load distribution for all connected branches; and adjusting for a delay introduced by the inserted buffers (para 0071, 0073), uniformly distributing a capacitance of each branch of the nets at a corresponding branch point; determining a load at each branch point; and checking if a buffer inserted at each branch point is capable of handling the loaded determined for that branch point ((para 0071, 0073)).

(Claims 13-15) said method is embodied in a set of computer instructions stored on a computer readable media; said computer instructions, when loaded into computer, cause the computer to perform the steps of said method (fig 2); wherein said computer instruction are compiled computer instructions stored as an executable program on said computer readable media (fig 2), wherein said method is embodied in a set of computer readable instructions stored in an electronic signal (fig 2, insofar the limitation is understood).

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2. Claims 1-5, 7, 9, 13-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Ginneken (USP 6453446)

(Claims 1, 16-19)

preparing a physical hierarchy of the circuit design with placed macros (fig 10B-C);

performing global routing on the physical hierarchy (col 16 line 18+);

determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets (col 13 line 24-36);

calculating a position for each buffer (col 13 line 24-25); and

inserting a buffer configured to boost timing performance at each calculated position (col 13 line 24-36).

(Claims 2-3) wherein said buffers are inverters/repeaters (col 7-8, 13).

(Claims 4-5) identifying a set at least one edge in said nets for inserting buffers; and determining an optimal number of buffers to be inserted on each edge (fig 1-10), calculating, for each edge, the optimal number of buffers based on an optimal timing for the edge, a delay of the edge, and an impedance of the edge (fig 1-10).

(Claims 7, 9) determining a uniform load distribution for all connected branches; and adjusting for a delay introduced by the inserted buffers (col 1 line 22+, col 2 line 48+, col 9-11), uniformly distributing a capacitance of each branch of the nets at a corresponding branch point; determining a load at each branch point; and checking if a buffer inserted at each branch point is capable of handling the loaded determined for that branch point (col 1 line 22+, col 2 line 48+, col 9-11).

(Claims 13-15) said method is embodied in a set of computer instructions stored on a computer readable media; said computer instructions, when loaded into computer, cause the computer to perform the steps of said method (fig 1); wherein said computer instruction are compiled computer instructions stored as an executable program on said computer readable media (fig 1), wherein said method is embodied in a set of computer readable instructions stored in an electronic signal (fig 1, insofar the limitation is understood).

3. Claims 1-5, 13-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Le (USP 5995735)

(Claims 1, 16-19)

preparing a physical hierarchy of the circuit design with placed macros (fig 1-4);

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performing global routing on the physical hierarchy (col 3 line 21+);  
determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets (fig 1-4, col 1 line 41+);  
calculating a position for each buffer (abstract, background, summary, fig 1-4); and  
inserting a buffer configured to boost timing performance at each calculated position (abstract, background, summary, fig 1-4).

(Claims 2-3) wherein said buffers are inverters/repeaters (col 1, 3 fig 1-4).

(Claims 4-5) identifying a set at least one edge in said nets for inserting buffers; and  
determining an optimal number of buffers to be inserted on each edge (fig 1-4), calculating, for each edge, the optimal number of buffers based on an optimal timing for the edge, a delay of the edge, and an impedance of the edge (fig 1-4).

(Claims 13-15) said method is embodied in a set of computer instructions stored on a computer readable media; said computer instructions, when loaded into computer, cause the computer to perform the steps of said method (col 6); wherein said computer instruction are compiled computer instructions stored as an executable program on said computer readable media (col 6), wherein said method is embodied in a set of computer readable instructions stored in an electronic signal (col 6, insofar the limitation is understood).

4. Claims 1-5, 7, 9, 13-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Boyle et al (US Patent Application No. 20010010090)

(Claims 1, 16-19)

preparing a physical hierarchy of the circuit design with placed macros (para 0011);  
performing global routing on the physical hierarchy (fig 7B, para 0092-0093, 0100-0102, 0106-0107);

determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets (para 0038, 0045, 0055-0056, 0060-0061, 0095, 0097, 0104-0105);

calculating a position for each buffer (para 0080, fig 5, 7); and  
inserting a buffer configured to boost timing performance at each calculated position nets (para 0038, 0044-0045, 0055-0056, 0060-0061, 0095, 0097, 0104-0105).

(Claims 2-3) wherein said buffers are inverters/repeaters (para 0055-0056, 0080, 0095, 0097, 0104).

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(Claims 4-5) identifying a set at least one edge in said nets for inserting buffers; and determining an optimal number of buffers to be inserted on each edge (fig 2-7), calculating, for each edge, the optimal number of buffers based on an optimal timing for the edge, a delay of the edge, and an impedance of the edge (fig 2-7).

(Claims 7, 9) determining a uniform load distribution for all connected branches; and adjusting for a delay introduced by the inserted buffers (para 0057, 0061, 0066, 0073), uniformly distributing a capacitance of each branch of the nets at a corresponding branch point; determining a load at each branch point; and checking if a buffer inserted at each branch point is capable of handling the loaded determined for that branch point (para 0057, 0061, 0066, 0073).

(Claims 13-15) said method is embodied in a set of computer instructions stored on a computer readable media; said computer instructions, when loaded into computer, cause the computer to perform the steps of said method (fig 4, para 0033, claim 30); wherein said computer instruction are compiled computer instructions stored as an executable program on said computer readable media (fig 4, para 0033, claim 30), wherein said method is embodied in a set of computer readable instructions stored in an electronic signal (fig 4, para 0033, , claim 30, insofar the limitation is understood).

#### ***Allowable Subject Matter***

Claims 6 and 8 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6, 8, and 10-12 would be allowable because the prior art does not teach or suggest the limitations in claim 6, claim 8, and claim 10.

#### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh

Patent Examiner

Paul Dinh  
3/9/05